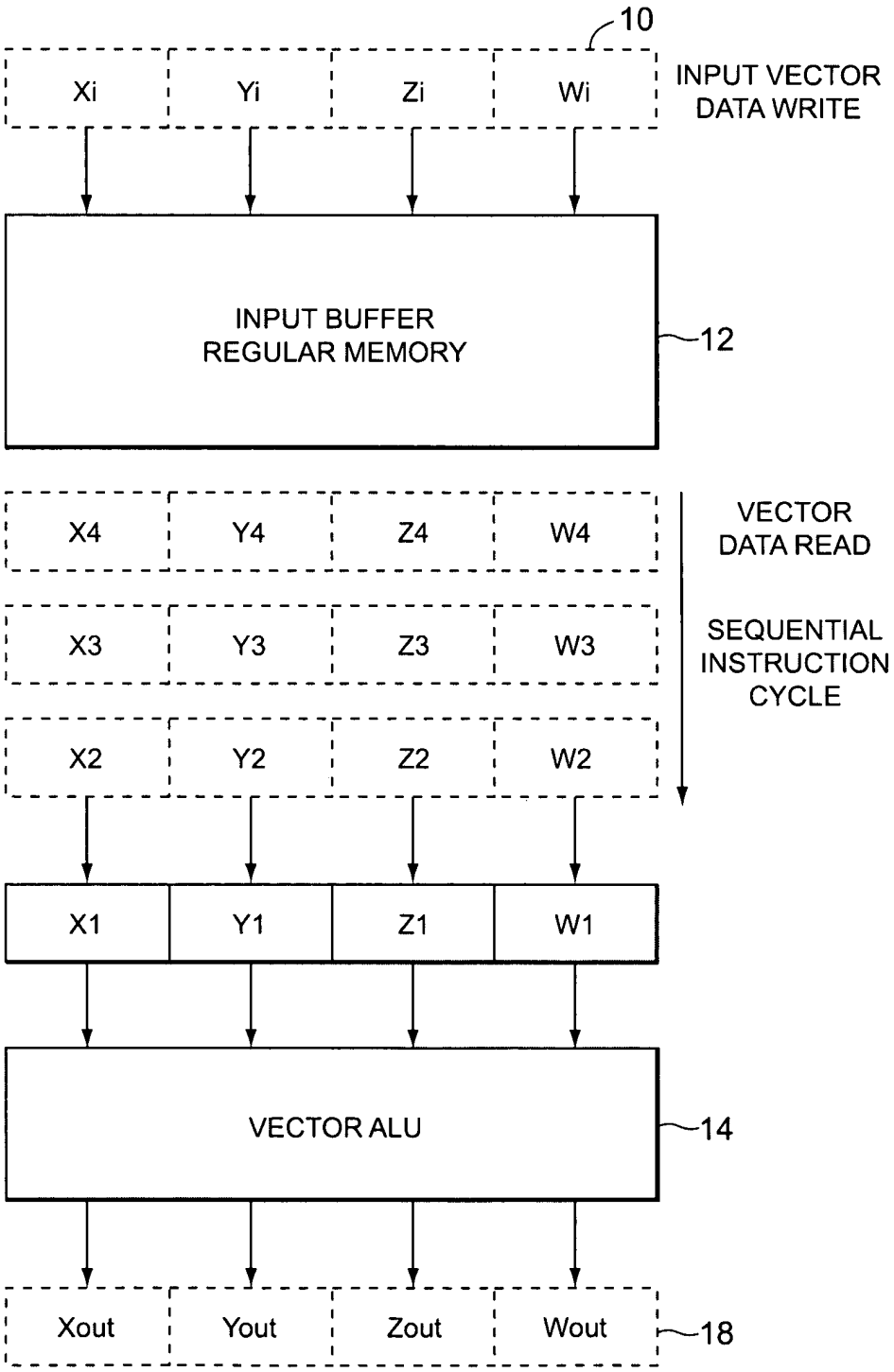

FIG. 1

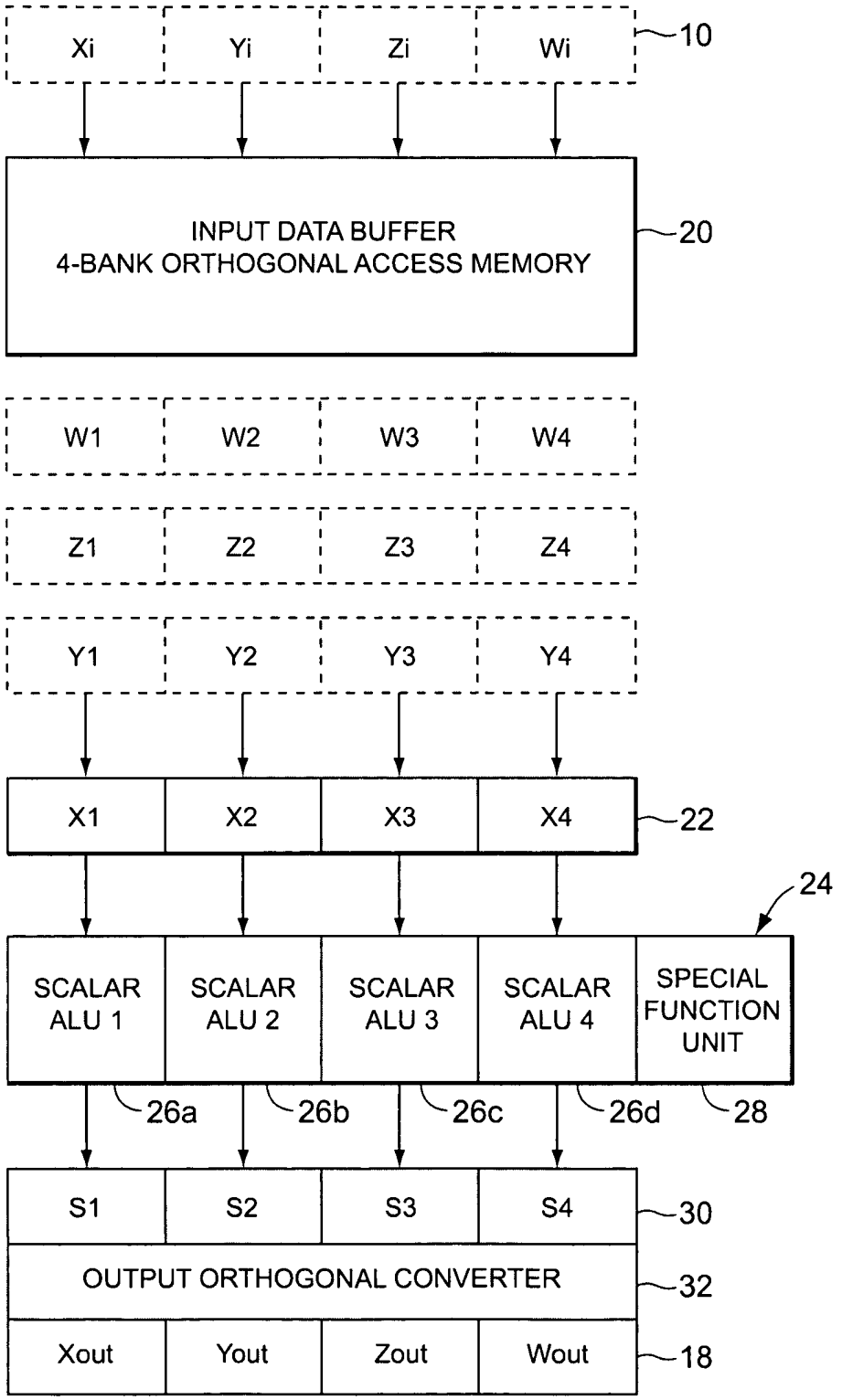
Xi
Yi
Zi
Wi
10
INPUT DATA BUFFER
4-BANK ORTHOGONAL ACCESS MEMORY
20
W1
W2
W3
W4
Z1
Z2
Z3
Z4
Y1
Y2
Y3
Y4
X1
X2
X3
X4
22
24
SCALAR ALU 1
SCALAR ALU 2
SCALAR ALU 3
SCALAR ALU 4
SPECIAL FUNCTION UNIT
26a
26b
26c
26d
28
S1
S2
S3
S4
30
OUTPUT ORTHOGONAL CONVERTER
32
Xout
Yout
Zout
Wout
18

FIG. 2

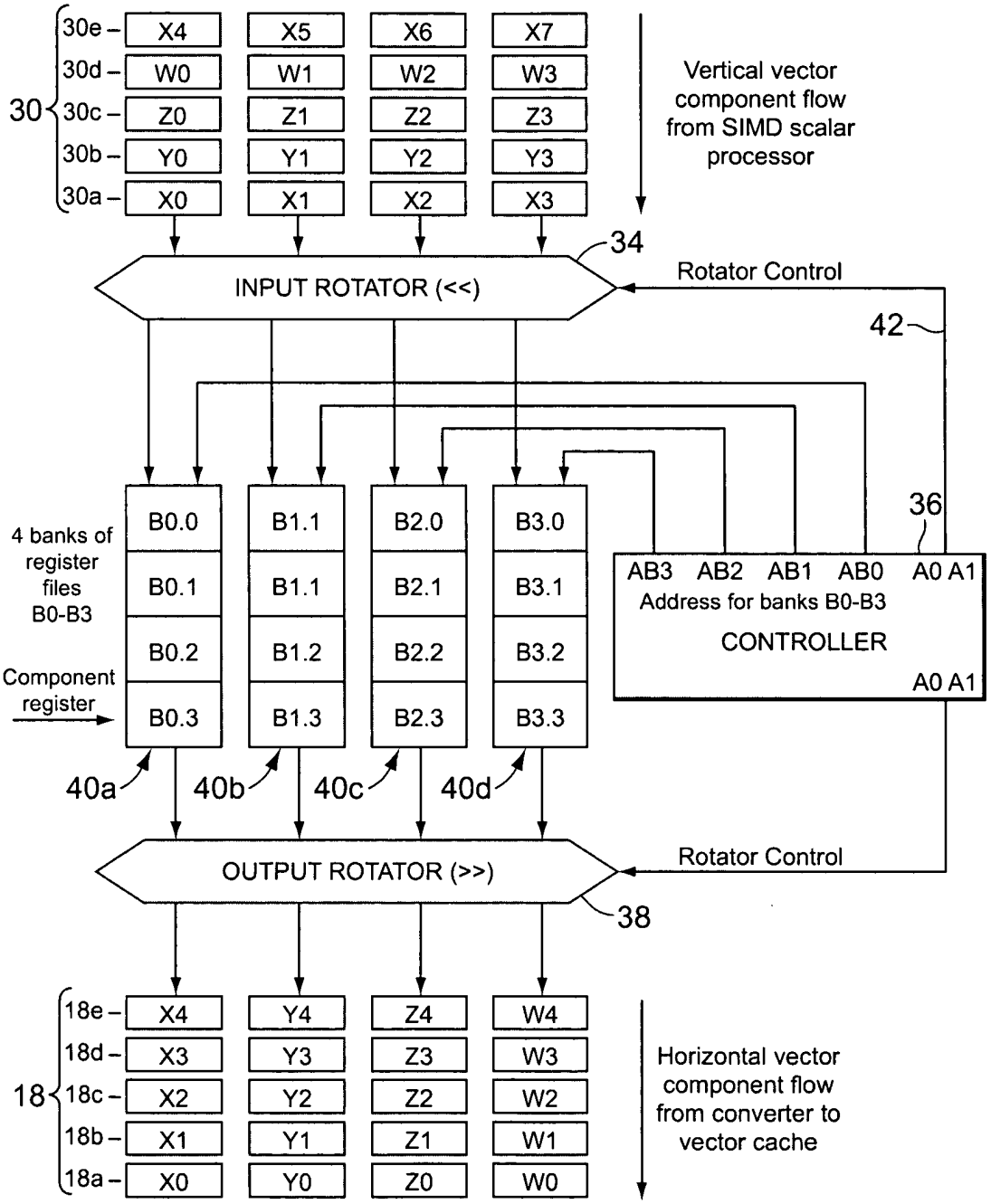
30
30e
30d
30c
30b
30a
X4
X5
X6
X7
W0
W1
W2
W3
Z0
Z1
Z2
Z3
Y0
Y1
Y2
Y3
X0
X1
X2
X3
Vertical vector component flow from SIMD scalar processor
34
INPUT ROTATOR (<<)
Rotator Control
42
36
4 banks of register files B0-B3
Component register
B0.0
B0.1
B0.2
B0.3
B1.1
B1.1
B1.2
B1.3
B2.0
B2.1
B2.2
B2.3
B3.0
B3.1
B3.2
B3.3
AB3 AB2 AB1 AB0 A0 A1
Address for banks B0-B3
CONTROLLER
A0 A1
40a
40b
40c
40d
OUTPUT ROTATOR (>>)
Rotator Control
38
18
18e
18d
18c
18b
18a
X4
X3
X2
X1
X0
Y4
Y3
Y2
Y1
Y0
Z4
Z3
Z2
Z1
Z0
W4
W3
W2
W1
W0
Horizontal vector component flow from converter to vector cache

FIG. 3

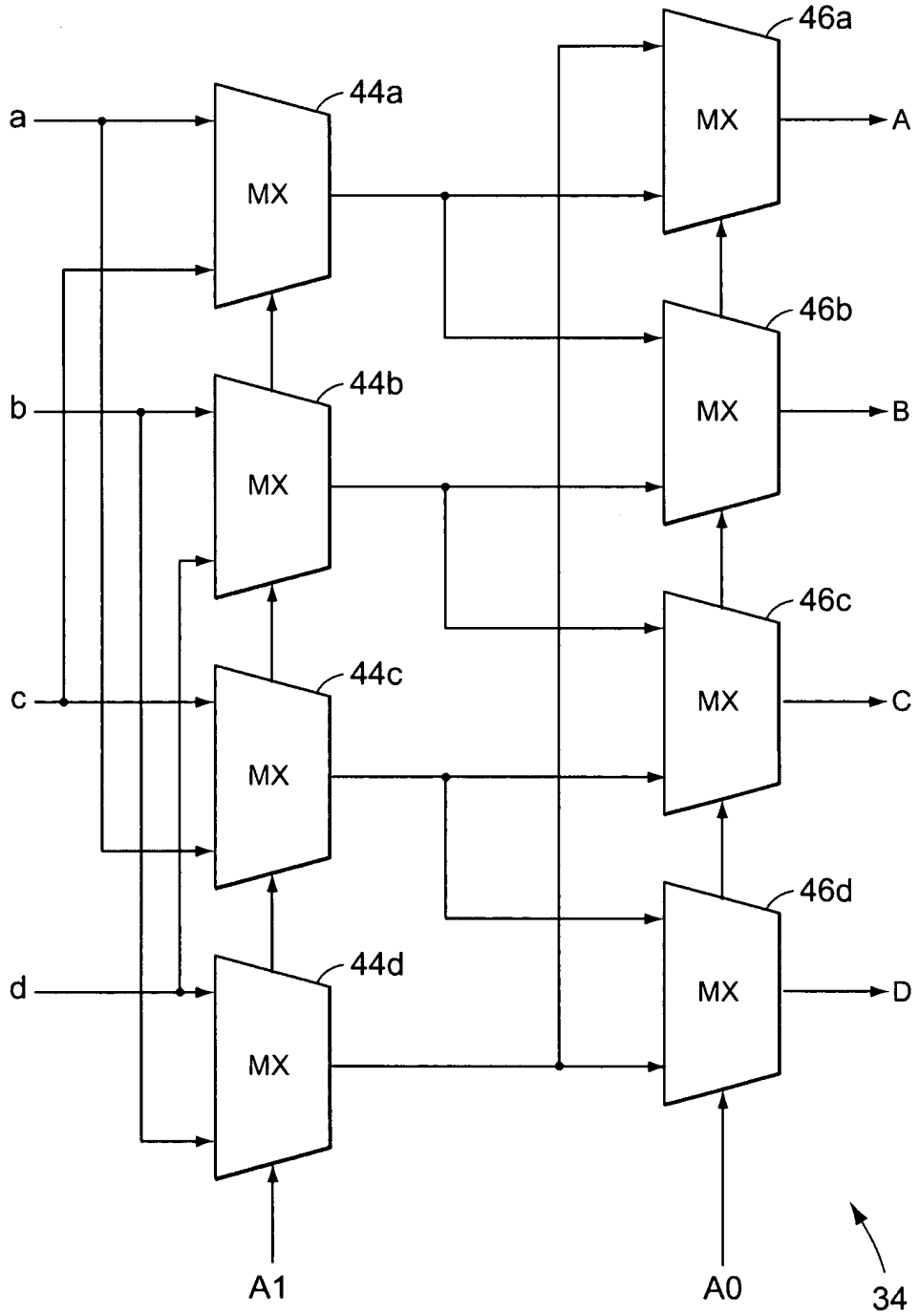

FIG. 4

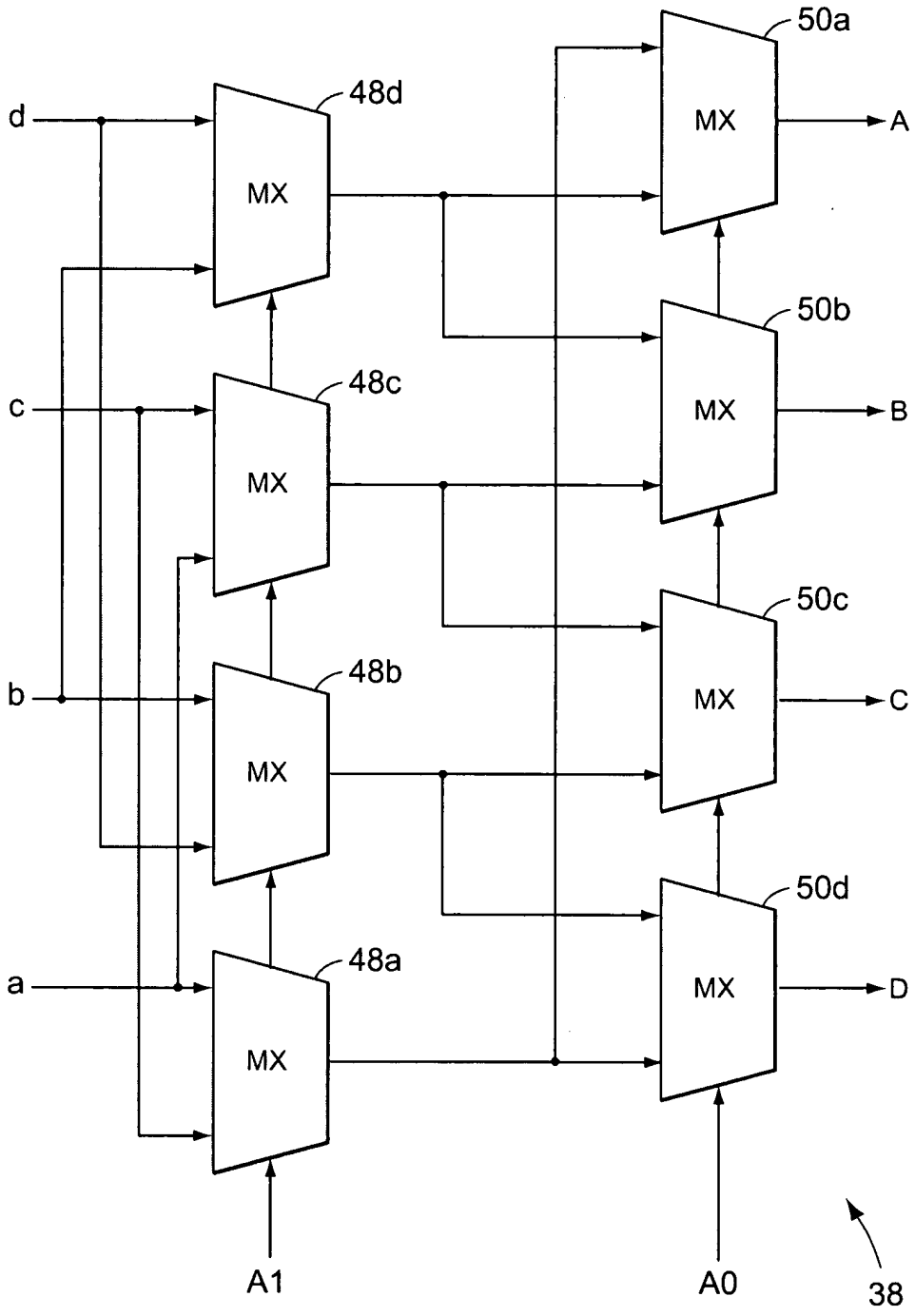

FIG. 5

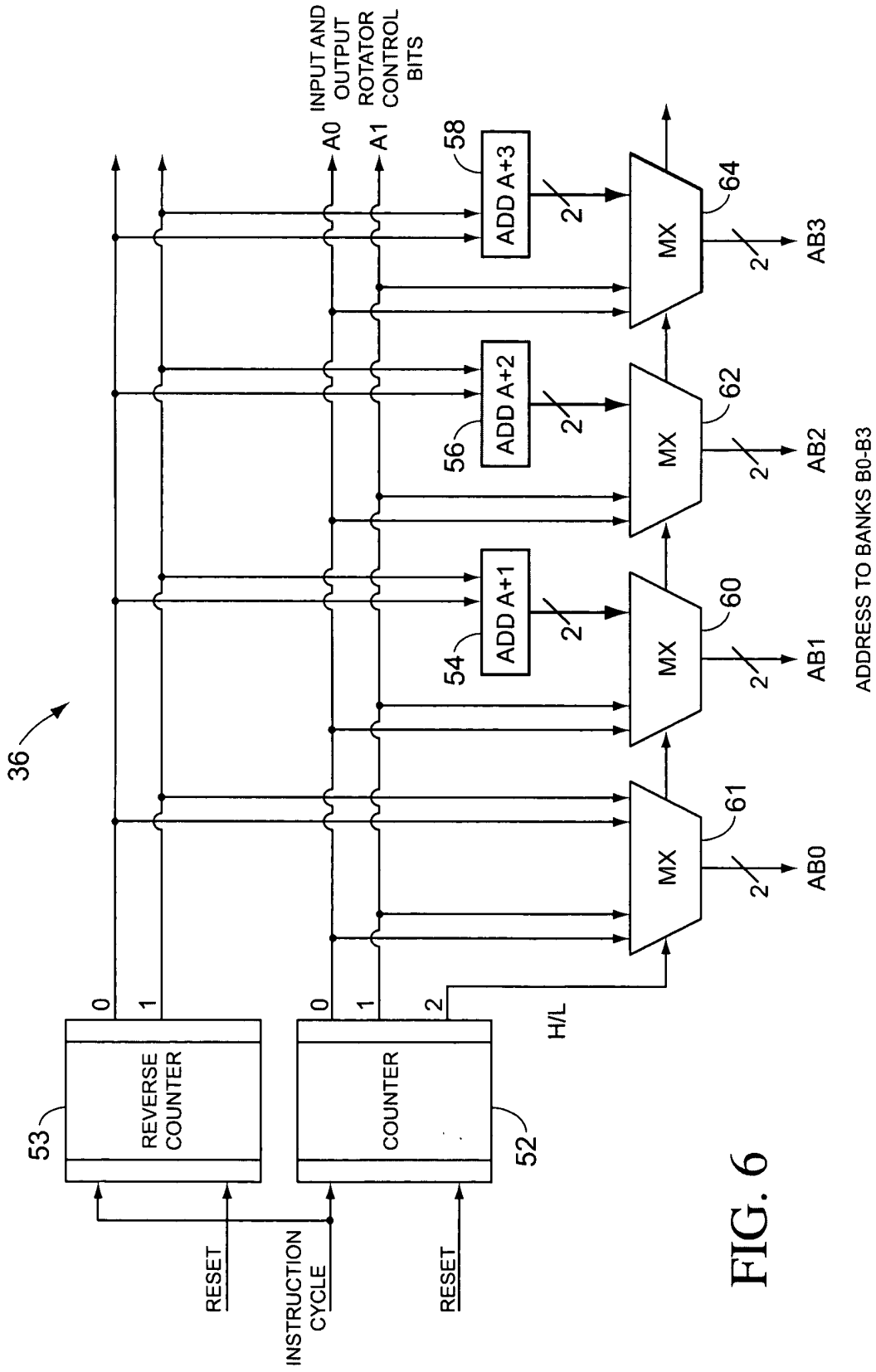
INPUT AND OUTPUT ROTATOR CONTROL BITS
A0
A1
58
ADD A+3
56
ADD A+2
54
ADD A+1
MX
64
62
60
61
AB3
AB2
AB1
AB0
2
ADDRESS TO BANKS B0-B3
36
REVERSE COUNTER
53
COUNTER
52
0
1
2
H/L
RESET
INSTRUCTION CYCLE
RESET

FIG. 6

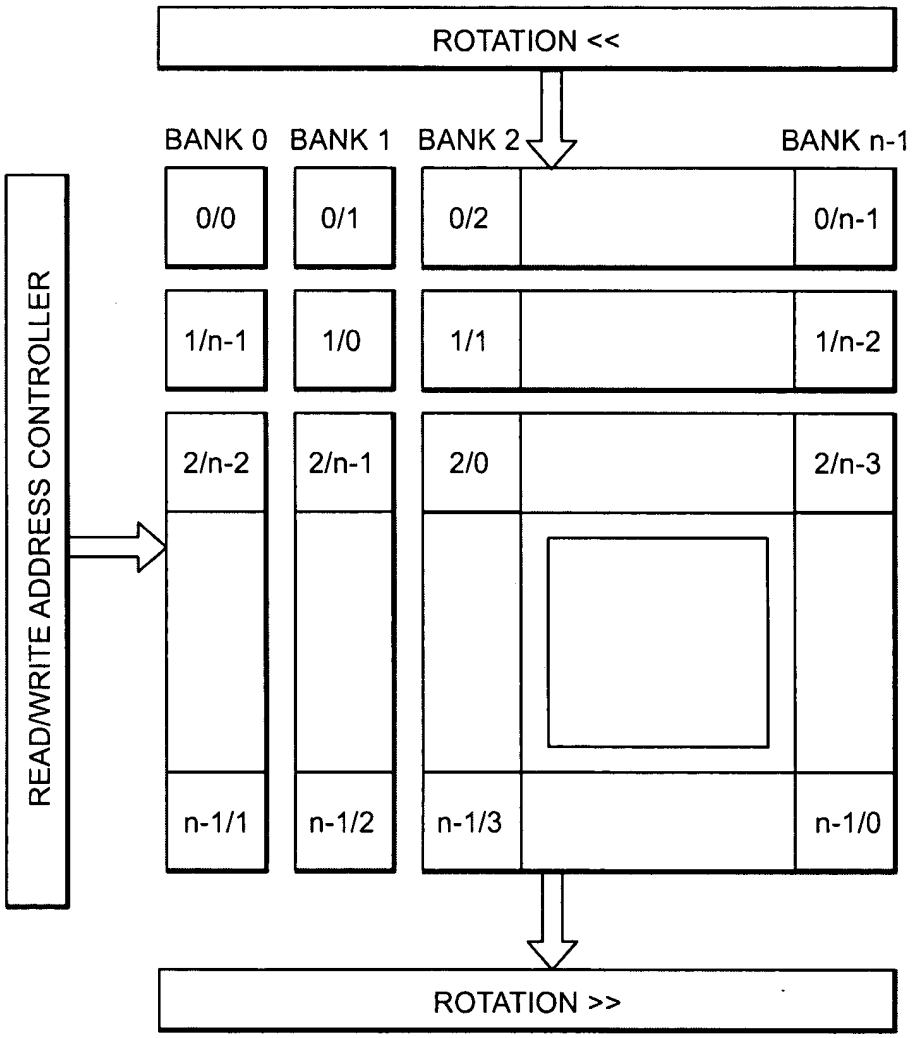
ROTATION <<
BANK 0
BANK 1
BANK 2
BANK n-1
0/0
0/1
0/2
0/n-1
1/n-1
1/0
1/1
1/n-2
2/n-2
2/n-1
2/0
2/n-3
n-1/1
n-1/2
n-1/3
n-1/0
READ/WRITE ADDRESS CONTROLLER
ROTATION >>

FIG. 7

Cycle	AB0	AB1	AB2	AB3	Input vector components in order B0, B1, B2,B3	Rotate Input	Output vector components in order B0, B1, B2, B3	Rotate Output
1	0	0	0	0	X0 X1 X2 X3	NO	INVALID	NO
2	1	1	1	1	Y3 Y0 Y1 Y2	>>1	INVALID	
3	2	2	2	2	Z2 Z3 Z0 Z1	>>2	INVALID	
4	3	3	3	3	W1 W2 W3 W0	>>3	INVALID	
	AB0	AB0	AB0	AB0				
5	0	1	2	3	X4 X5 X6 X7	NO	X0 Y0 Z0 W0	NO
6	3	0	1	2	Y7 Y4 Y5 Y6	>>1	W1 X1 Y1 Z1	<<1
7	2	3	0	1	Z6 Z7 Z4 Z5	>>2	Z2 W2 X2 Y2	<<2
8	1	2	3	0	W5 W6 W7 W4	>>3	Y3 Z3 W3 X3	<<3
	AB0	AB0+1	AB0+2	AB0+3				
9	0	0	0	0	X8 X9 X10 X11	NO	X4 Y4 Z4 W4	NO
10	1	1	1	1	Y11 Y8 Y9 Y10	>>1	W5 X5 Y5 Z5	<<1
11	2	2	2	2	Z10 Z11 Z8 Z9	>>2	Z6 W6 X6 Y6	<<2
12	3	3	3	3	W9 W10 W11 W8	>>3	Y7 W7 Z7 X7	<<3
	AB0	AB0	AB0	AB0				

FIG. 8